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Improved Parylene-packaged Pentacene Thin-film Transistors

Hsi-wen Lo and Yu-Chong Tai

Department of Electrical Engineering, California Institute of Technology, Pasadena, California, 91125, USA

This paper presents improved parylene-packaged thin-film transistors. Several spin-cast dielectrics were investigated to improve the surface roughness of parylene. The corresponding mobility and performance of pentacene thin film transistors were also reported. The relation between pentacene grain sizes and roughness of surfaces where pentacene grows were also investigated. To further improve the mobility, micromachined shadow masks made of silicon and parylene were employed to define the source and drain contacts. The improved pentacene thin-film transistor has a mobility of 0.2 cm^2/V-s and an on/off ratio of 10^4.

Introduction

Vision loss due to retinitis pigmentosa (RP) and age-related macular degeneration (AMD) has troubled millions of people around the world. Recently, a retinal prosthesis has been developed for the treatment of aged-related blindness. This technology is based on the concept of replacing photoreceptor function with an electronic device (1). For this technology, a huge amount of electrodes are needed to achieve reasonable or high resolutions. A biocompatible and scalable high lead count electrode array for retinal prosthesis has been successfully fabricated (2). These electrodes are directly connected to the implanted control electronics through metal interconnects. As the resolution increase, the number of electrodes and interconnects increase, too. So is the volume of the implanted device. One way to reduce the number of metal interconnects and to satisfy the small volume constraint is to introduce a multiplexer into the system. This multiplexer has to overcome such difficulties as the corrosive environment and integration with the metal interconnects and so on.

One revolutionary approach to solve the problem is to explore biocompatible electronics that do not require conventional hermetic packaging and, at the same time, flexible enough for implantation use.

The combination of organic semiconductor and polymer substrate can serve this purpose. Pentacene ($C_{14}H_{22}$) thin film transistors (TFT) have been fabricated and possess a hole mobility up to 2.59 cm^2/V-s (3), which is comparable to the popular a-Si:H TFT technology.

Pentacene, however, is sensitive to oxygen, so unprotected pentacene transistors are vulnerable to even normal environments. It is therefore interesting to use parylene (readily a proven biocompatible material) as a pentacene-protecting polymer. Parylene C, a widely used MEMS (micro-electro-mechanical system) material, shows great flexibility (Young's modulus ~ 4 GPA), chemical inertness and biocompatibility (4). Parylene C has

been recognized as a USP Class VI material and its intraocular biocompatibility has been studied (2).

Previously, we demonstrated the first flexible parylene-pentacene electronics where parylene is exclusively used as the substrate, gate insulator and encapsulation layer (5). This device took bottom contact configurations and used parylene as gate dielectrics. However, with all our due effort, the mobility of pentacene was limited to the order of 0.01 cm^2/V-s ranges. To improve the mobility, and therefore the overall performance of parylene packaged thin-film transistors, we performed a systematic research.

Surface Roughness and Pentacene Grain Growth

It is known that pentacene mobility is closely related to the surface properties. One of the most important factors that affect pentacene grain growth is the surface roughness (6). For this reason, we studied the surface roughness of parylene with various thicknesses. Parylene was deposited on clean silicon wafers with a room temperature chemical vapor deposition (CVD) process. Prior to deposition, silicon wafers were all cleaned with piranha solution followed by diluted hydrofluoric acid dipping. The thickness of parylene was determined by controlling the weight of parylene dimmers. Veeco Digital Instrument Dimension 3100 scanning probe microscope, or atomic force microscope (AFM) was used to measure the surface roughness. Root mean square roughness was calculated with the software that comes with the AFM. Figure 1 shows the AFM picture of 10μm parylene C and 0.2 μm parylene.

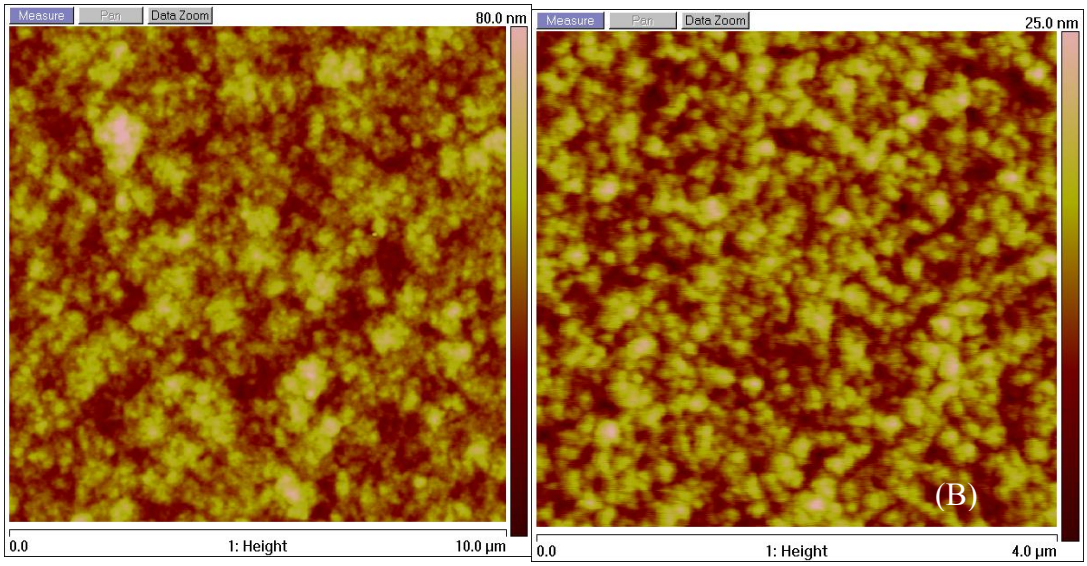

Figure 1. AFM images of untreated parylene. (a) 10μm thick, (b) 0.2μm thick.

The root mean square roughness, R_q, is 9.65nm and 3.52nm, for 10μm and 0.2μm samples, respectively. In order to show that surface roughness of parylene alone plays an important role for pentacene grains, we fabricated a flat parylene surface via a flipping method. Since parylene coating is extremely conformal and the surface roughness of commercial silicon wafers is usually in the range of a few angstroms, the flat and smooth surface can be achieved by depositing parylene on silicon wafers. The process is illustrated in Figure 2 and the AFM image of the so fabricated parylene film is also shown.

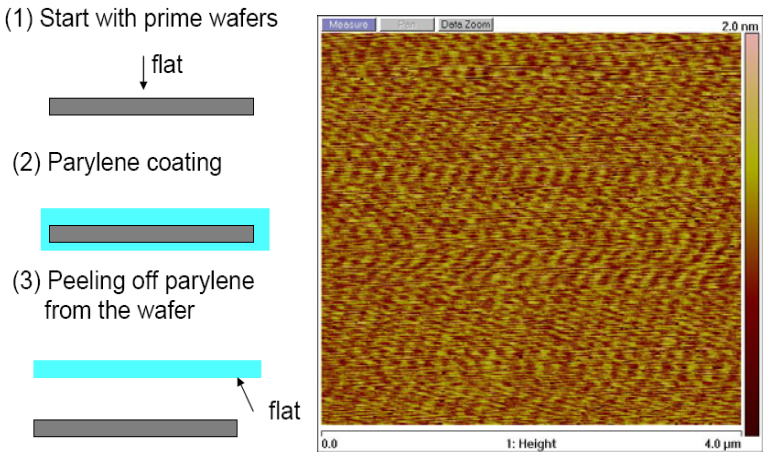

Figure 2. Left: illustrated fabrication of flat parylene. Right: AFM image of flat parylene (only noise was measured.)

Without any treatment, pentacene was thermally evaporated onto both parylene samples and AFM images were obtained, as shown in Figure 3

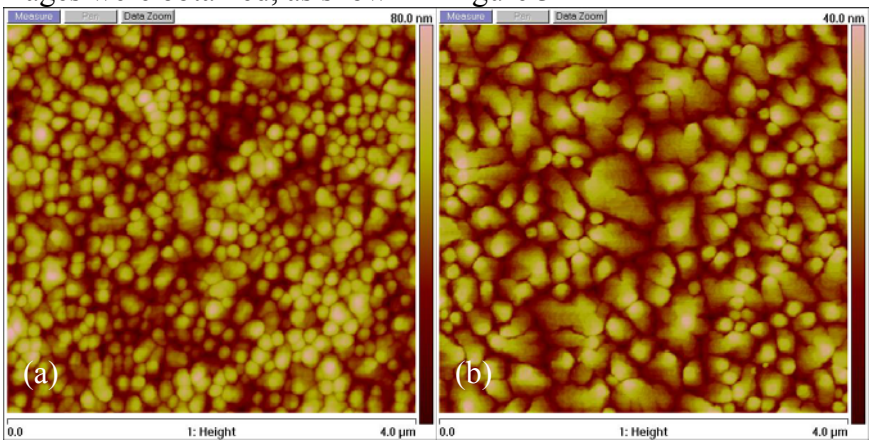

Figure 3. AFM images of pentacene on flat parylene (a) and untreated parylene (b).

As can be seen from Figure 3, the grain sizes of pentacene on flat parylene and untreated parylene differ a lot. It follows that, to improve our transistor performance, the surface roughness of parylene must be reduced. To reduce the surface roughness, we cover parylene surfaces with several spin-cast dielectrics, including polyvinylphenol (PVP), SU-8, and PMMA. Surface roughness of these spin-cast dielectrics were measured with AFM and average grain diameters of pentacene grains evaporated on these surface were calculated with Scion Image software. Table I summarizes the surface roughness and sizes of pentacene grains on smoothened parylene surfaces and Figure 4 shows pentacene grains on these dielectrics.

As can be seen from Table I, native parylene surface is rough and cannot produce large grains of pentacene. Therefore, it is required to spin-cast thin dielectric layers on parylene surface to have smooth surfaces and thus larger pentacene grains and better transistor performances.

Table I. Grain diameters of pentacene on various surface of different roughness.

Smoothing Layer	None	495 PMMA A2(1krpm, 40seconds)	495 PMMA A2(0.5krpm,40 seconds)	PVP (5%, 3krpm, 40 seconds)	PVP(10% +5%CLA, 1krpm,40 seconds)	SU8-2(5k rpm)
Substrate	0.2μm parylene	0.2μm parylene	10μm parylene	0.2μm parylene	10μm parylene	10μm parylene
Ts	0	967Å	1400Å	1300Å	5600Å	9600Å
Ra	2.81nm	0.52nm	0.755nm	0.984nm	0.486nm	0.325nm
Rq	3.52nm	0.65nm	0.960nm	1.23nm	0.382nm	0.409nm
Grain dia.	0.378μm	0.852μm	0.941μm	0.559μm	0.742μm	0.680μm

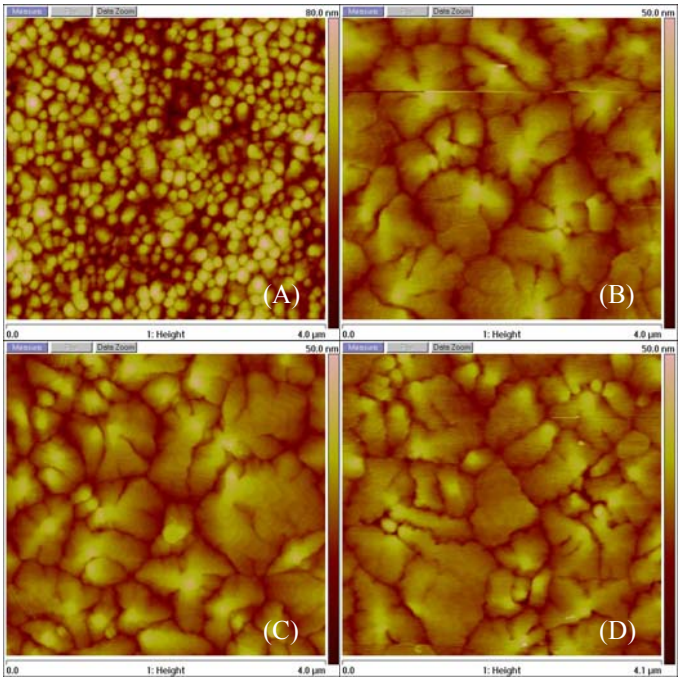

Figure 4. AFM images of Pentacene grains on naked parylene (A), PMMA (B), PVP (C) and SU8-2 (D).

Micromachined Shadow Masks and Top Contact Configuration

Aside from surface roughness problems, the low mobility of our previous devices also results from bottom-contact configuration. It is well known that top contact configuration gives better transistor performance than bottom contact configuration. However, top source and drain contacts can only be fabricated with shadow masks since pentacene is incompatible with organic solvents widely used in conventional photolithography processes.

To achieve high turn-around time and flexibility of design, we use two-side DRIE process to fabricate shadow masks out of silicon wafers. Figure 5 shows the illustrated process and fabricated silicon shadow mask.

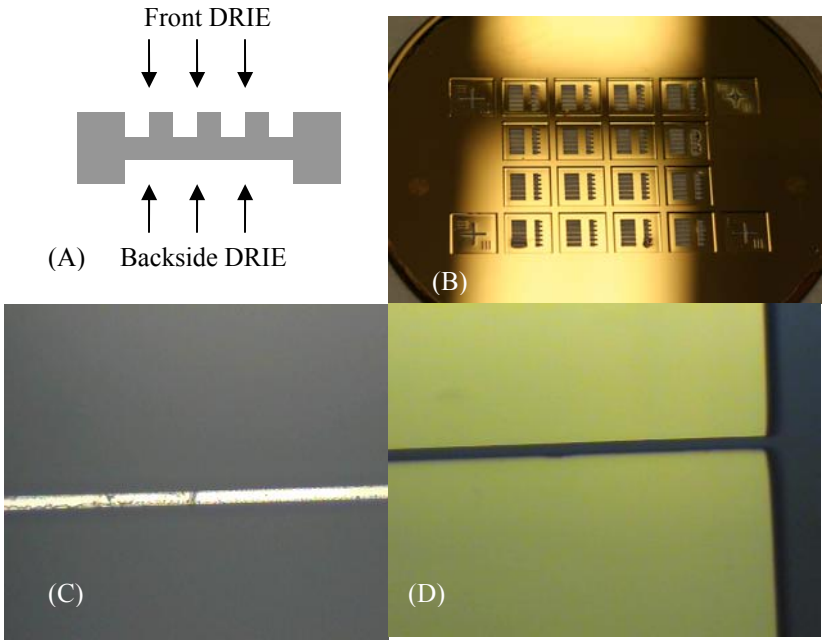

Figure 5. Illustrated two-side DRIE process (A), fabricated silicon shadow mask (B), 20-μm shadow mask beam (C), Au electrodes with 20-μm gap, fabricated with this shadow mask.

Electrode with 20-μm gaps can be consisistenly and reliably fabricated with the use of this silicon shadow mask. Although silicon shadow masks fabricated with two-side DRIE processes provide excellent control over channel lengths, it still takes too long to fabricate and DRIE processes are costly. In lieu of silicon, we turned to parylene shadow masks.

As mentioned above, parylene is an excellent and widely used MEMS structural material and the etch rate of oxygen plasma on parylene is around 0.5μm/min. Compared to fabrication of silicon shadow masks, fabrication of parylene ones is much easier and time and cost saving since it requires only one-side process and RIE oxygen plasma. The fabrication of parylene shadow masks starts with depositing a layer of sacrificial material, be it photoresist or chromium, on silicon wafers. 30-μm Parylene C is deposit. Al is then deposited and patterned as parylene etching mask. RIE oxygen plasma is used to etch parylene. After etching, Al and the sacrificial layer are removed, rendering a parylene shadow mask.

Figure 6 shows the illustrated process and the fabricated parylene shadow masks. Because of parylene's flexible ability, the minimum channel gap that can be achieved consistently is around 50-μm. Using parylene shadows masks provides additional benefits that there is no worry that shadow masks will scratch pentacene surfaces and that it is easy to handle and align.

Transistor Performance

To correctly assess the effects of smoothing layers and top-contact and to reach an optimal improving solution, we fabricated pentacene transistors with different smoothing

layers and used top-contact configuration and bottom-contact configuration. The results are summarized in Table II. Detailed fabrication processes can be found in (5)

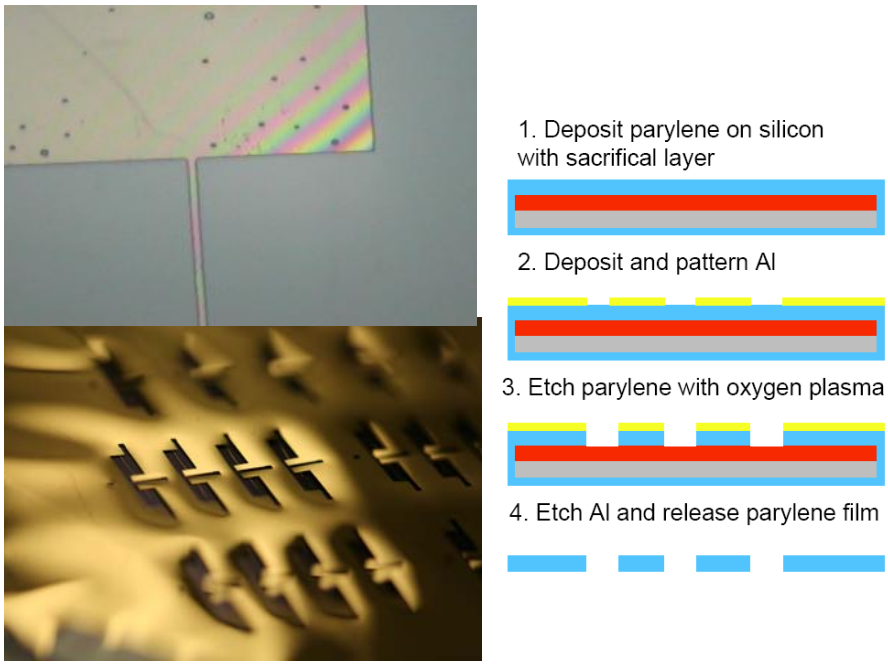

Figure 6. Right : illustrated process. Left: pictures of fabricated parylene shadow masks. The bridget in the top-left picture is 50μm wide.

Table II. Transistor performances using different smoothing layers and top/bottom-contact configuration.

Contact configuration	**Bottom contact**		**Top contact**		
Gate insulator	0.2μm parylene	0.2μm parylene	0.2μm parylene	0.2μm parylene	0.2μm parylene
Smoothing layer	None	Wt 10% PVP + 10%CLA in PGMEA	None	Wt 5% PVP, 3krpm	495 PMMA A2, 1krpm
Mobility (cm^2/V-s)	0.02	0.02	0.04	0.2	0.2

As can be seen from Table II, smoothing layers boost the mobility of transistors up one order of magnitude. For transistors with smoothing layers, top contact configurations do provide better mobilities. Meanwhile, for transistors without smoothing layers, top contact and bottom contact produce no significant differences. The latter can be explained by the metal suppression effect on pentacene grain growth (7). In all, to have decent mobilities for most bio-implant applications, smoothing layers and source/drain of top contact configuration are required for parylene packaged pentacene thin-film transistors.

Conclusion

The effect of surface roughness of parylene on pentacene grain growth and performance of pentacene thin-film transistors has been explored. Spin-cast dielectrics are used to produce smooth parylene surfaces. To further improve mobility, top-contact configuration is also used. Micromachined silicon and parylene shadow masks are used

as shadow masks for top-contact source/drain electrodes. The improved parylene packaged pentacene thin-film transistors have a decent mobility of 0.2 cm^2/V-s.

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